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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/635,378	08/06/2003	Chunsuk Suh	8028-4 DIV (SPX200006-006	1282

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EXAMINER	
IM, JUNGHWA M	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/635,378	SUH, CHUNSUK	
	Examiner	Art Unit	
	Junghwa M. Im	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *5-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 5-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narui et al. (US 6150689), hereinafter Narui in view of Liu et al. (US 6291335), hereinafter Liu.

Regarding claim 5, Fig. 3 of Narui shows a device through using a method of manufacturing a semiconductor memory device, comprising the steps of (Figures 6-27):

a) forming gate electrodes (8A) on a substrate (1) having a cell region and a periphery region;

b) forming a first insulating layer (18, 19) over the substrate, the first insulating layer covering the gate electrodes (Fig. 10);

c) forming first contact holes (24, 25, 26) and stud holes (20) in the first insulating layer;

d) forming contact studs and first contact portions in the stud holes and the first contact holes, respectively ;

e) forming a second insulating layer (31) on the first insulating layer and on the contact studs;

f) forming a bit line contact holes (23) passing through the first and second insulating layers;

g) forming bit line contacts in the bit line contact holes; and

h) forming bit lines (BL_1, BL_2) on the second insulating layer.

Narui discloses most aspect of the instant invention except forming metal studs and metal contact holes. Liu discloses formation of tungsten in the contact holes (col.5, lines 31-34).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Liu into the device of Narui in order to form the metal contact holes and the metal studs in lieu of polysilicon to improve the conductivity.

Regarding claim 6, Fig. 3 of Narui shows a device made through further comprising the steps of :

i) forming a capacitor over the cell region (C) of the substrate;

j) forming a third insulating layer (32) over the substrate, said third insulating layer covering the bit lines;

k) forming second contact holes (36) in the second and third insulating layers, the second contact holes exposing a portion of the contact studs; and

1) forming second contacts in the second contact holes.

Narui discloses most aspect of the instant invention except forming the metal studs and the metal contact holes. Liu discloses formation of tungsten in the contact holes (col.5, lines 31-34).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Liu into the device of Narui in order to

form the metal contact holes and the metal studs in lieu of polysilicon to improve the conductivity.

Regarding claim 7, Fig. 3 of Narui shows a device further comprising the steps of forming the stud holes further comprises the steps of: forming a first photoresist pattern on the first insulating layer; and etching the stud holes in the first insulating layer using the first photoresist pattern as a mask, wherein after the stud holes are formed, the first photoresist pattern is removed (col.13, lines 20-35).

Regarding claim 8, Liu discloses a method wherein the first metal contact holes are formed using anisotropic etching processing to expose a portion of an active area and at least one of said gate electrodes (col.4, lines18-33).

Regarding claim 9, Fig. 3 of Narui shows a device wherein the step of (d) further comprises the steps of depositing a first conductive material layer on the first insulating layer, wherein said first conductive material layer fills the stud holes and the first metal contact holes; and removing a portion of the first conductive material layer to form the metal contact studs and the first metal contact portions (col. 20, lines 39-68).

Regarding claim 10, Fig. 3 of Narui shows a device wherein the step of (e) further comprising the step of planarizing the second insulating layer using a chemical mechanical polishing (CMP) technique (col. 19, lines 44-51).

Regarding claim 11, Fig. 3 of Narui shows a device wherein the step of (f) further comprises the steps of forming a second photoresist pattern on the second insulating layer; and etching the first and second insulating layers to form the bit line contact holes using the second photoresist pattern as a mask, wherein after the bit line contact holes are formed, the second photoresist pattern is removed (col. 21, lines 1-14).

Regarding claim 12, Fig. 3 of Narui shows a device wherein the step of (g) further comprises the steps of: depositing a second conductive material layer on the second insulating layer, the second conductive material layer filling the bit line contact holes; and removing a portion of the second conductive material layer on the second insulating layer (col. 10, lines 34-67).

Regarding claim 13, Fig. 3 of Narui shows a device wherein step (h) further comprises the steps of: depositing a third conductive material layer (44) on the second insulating layer, wherein the third conductive material layer contact the bit line contacts; and patterning the third conductive material layer to form the bit lines (41B).

Regarding claim 14, Fig. 3 of Narui shows an area of a lower portion of each metal contact stud is less than an area of an upper portion of each metal contact stud.

Regarding claim 15, Fig. 3 of Narui shows a device wherein step (k) further comprises the steps of: forming third photoresist patterns on the third insulating layer (39); etching the third insulating layer and the second insulating layer using the third photoresist patterns as a mask to form the second metal contact holes (36), wherein each of the second metal contact holes pass through between adjacent bit lines and exposes a portion of the metal contact studs.

Regarding claim 16, Fig. 3 of Narui shows a device wherein step (1) further comprises the steps of: depositing a fourth conductive material layer (33) on the third insulating layer (32), the fourth conductive material layer filling the second metal contact holes; and removing a portion of the fourth conductive material layer on the third insulating layer to form the second metal contacts (as discussed in claim 9).

Regarding claim 17, Fig. 3 of Narui shows a device wherein at least one of the bit line contacts is connected to active area (source/drain) of the substrate.

Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Narui and Liu as applied to claim 12 above, and further in view of Parekh et al. (US 6238971), hereinafter Parekh.

Regarding claim 18, the combined teachings of Narui and Liu show most aspect of the instant invention except "at least one of the bit line contacts is connected to one of the gate electrodes." Parekh discloses that bit line contacts to the gate (word line).

It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of Parekh into the device of Narui and Liu in order to have a bit line contacted to the gate to electrically couple the capacitor over the bit line.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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